REMARKS

Claims 1-11 are pending in the present application. Claims 1, 3-6 and 9-11 have been amended. Claims 5, 6, 9 and 10 have been withdrawn as being non-elected.

Drawings

Applicant notes the Examiner's acceptance of the drawings as filed along with the present application on February 5, 2002.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Claim Rejections-35 U.S.C. 112

Claims 3 and 4 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Although Applicant does not necessarily concede that original claims 3 and 4 are indefinite, claims 3 and 4 have been amended in an effort to more clearly define the features of the invention. Applicant respectfully submits that claims 3 and 4 are in compliance with 35 U.S.C. 112, second paragraph, and thus respectfully urges the Examiner to withdraw this rejection.

Claim Rejections-35 U.S.C. 102

Claims 1 and 2 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Jones et al. reference (U.S. Patent No. 6,117,778). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The method of manufacturing at least one semiconductor device on a substrate of claim 1 includes in combination "forming a resist pattern on the dielectric film, entirely covering the dielectric film in the effective device area and leaving at least part of the dielectric film exposed in the peripheral area, so that the exposed part of the dielectric film has an inner boundary that conforms with a shape of an outer boundary of the effective device area"; "etching the exposed part of the dielectric film"; "removing the resist pattern"; and "planarizing the dielectric film by chemical-mechanical polishing after the resist pattern has been removed". Applicant respectfully submits that the Jones et al. reference as relied upon by the Examiner does not disclose these features.

The Jones et al. reference as relied upon by the Examiner teaches methods of planarizing a dielectric layer formed on a wafer, wherein **a peripheral edge** of the dielectric film is etched prior to a CMP process. The method is described as primarily for removing an edge bead or lip which is generally formed as a circumferential ring about 2 to 8 mm in width from the edge of the wafer. That is, the Jones et al. reference merely merely discloses removing peripheral edges of dielectric 12 at portions 12a' and 12b', as illustrated in Fig. 1D. The peripheral portions of dielectric 12 are removed as

shown in Figs. 2A and 2B of the Jones et al. reference for example, wherein etchant 18 is sprayed from distribution conduit 17 over a circumferential edge of wafer 10, while wafer 10 is rotated on turntable 15.

Applicant respectfully submits that the Jones et al. reference does not define an effective device area. Accordingly, the Jones et al. reference does not disclose forming a resist pattern "so that the exposed part of the dielectric film has an inner boundary that conforms with a shape of an outer boundary of the effective device area", as featured in claim 1. Consequently, the Jones et al. reference does not disclose an etched part of a dielectric film having an inner boundary that conforms with a shape of an outer boundary of an effective device area. In the Jones et al. reference, only a peripheral edge or circumferential ring of the dielectric is etched. Since only a peripheral edge is removed in the Jones et al. reference, and not an area that conforms with an effective device area, the process of the Jones et al. reference would not effectively remove an adequate amount of dielectric film from a peripheral area of a wafer, and the dielectric film along the entirety of the wafer including an effective device area would not subsequently be satisfactorily planarized. Applicant therefore respectfully submits that the method of manufacturing of claim 1 distinguishes over the Jones et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1-3, is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 7 and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Jones et al. reference. Also, claim 11 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Jones et al. reference, in further view of the Watanabe reference (U.S. Patent No. 5,578,402). Applicant respectfully submits that the references as herein relied upon do not overcome the above noted deficiencies of the Jones et al. reference as noted above with respect to claim 1. The Examiner is therefore respectfully requested to withdraw the above noted respective rejections.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to acknowledge that claims 1-4, 7, 8 and 11 are allowed.

Also, since claims 1, 2 and 11 should be considered generic as asserted in the Response to Election/Restriction dated July 16, 2003, the Examiner is respectfully requested to rejoin non-elected claims 5, 6, 9 and 10, which should also be found allowable. The Examiner is therefore respectfully requested to pass all the claims of the present application to issue.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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